DIGITAL LOGIC FAMILIES

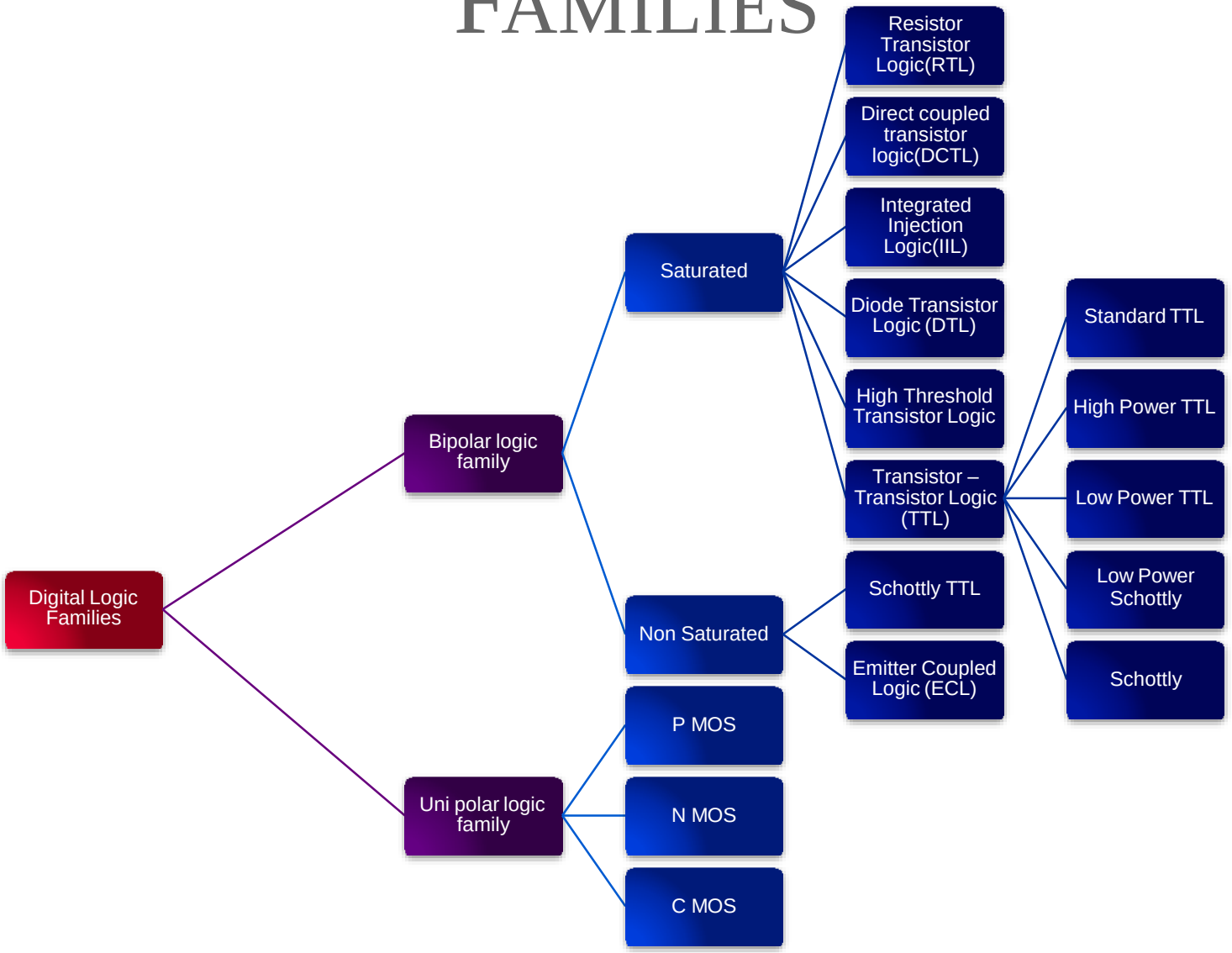
overview

- Introduction.
- Characteristics.
- Resistor Transistor Logic.
- Diode Transistor Logic.
- Transistor-Transistor Logic.
- Emitter coupled Logic.

1. INTRODUCTION

- Logic gates are available in the form of Integrated circuit(IC's)
- As per the level of integration, the IC's can accommodate more number of logic gates and digital functions.
- These forms are referred as logic family

2.Classification of Logic Families



3. IMPORTANT POINTS

- The digital familiy is categorized by two types (i)Bipolar and (ii) Unipolar
- In Saturated Bipolar logic families, the transistor in the IC driven in to saturation. In Non Saturated Bipolar logic families, the transistor in the IC not driven in to saturation
- In PMOS & NMOS Unipolar logic family only P & N channel MOSFETs are used. CMOS Unipolar logic family both P& N- channel MOSFETs are used.
- All family same logic level & same Voltage.

4. LEVEL OF INTEGRATION

- Number of gates fabricated in single IC
- There are 4 generation
  - Small Scale Integration (SSI) = 12 gates in 1 Chip
  - Medium Scale Integration (MSI) = 12 to 100 gates
  - Large Scale Integration(LSI)= 100 to 1000 gates
  - Very Large Scale Integration(VLSI)= Up to 1,00,000 or more

5. Specification of Digital IC's

- Different types of ICs are manufactured, based on the components used and their interconnections.
- These ICs are compared using certain performance specifications.

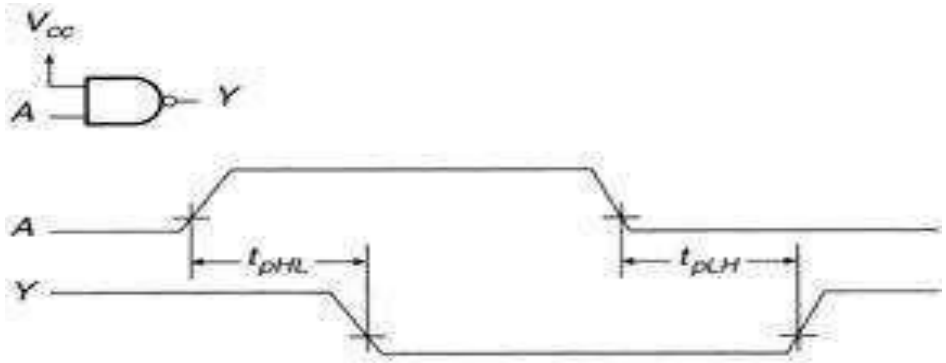
1. **Power Dissipation**
2. **Propagation Delay**
3. **Fan-In**
4. **Fan-Out**
5. **Input Logic Level**
6. **Output Logic Level**
7. **Compatibility**
8. **Noise Margin**
9. **Speed – Power Product**

1. Power Dissipation

- This is **the mean power of logic circuit draws from the supply** during one complete cycle.
- This parameter is very important because if the power dissipation is large, then the life period of the IC is reduced.
- It should be noted that in one complete cycle, the IC is in logic ‘1’ for half the time and in logic ‘0’ during the remaining half.
- The power dissipation of a logic gate is equal to the de supply voltage (V_{CC}) times the average supply current I_C).

2. Propagation Delay

- This parameter characterizes the **speed of a logic circuit**.
- The propagation delay of IC is the mean time required for a pulse to pass through the IC.
- It is thus defined as the time interval between a change in input and the resulting change in the output of an IC.
- It is represented by t_p.



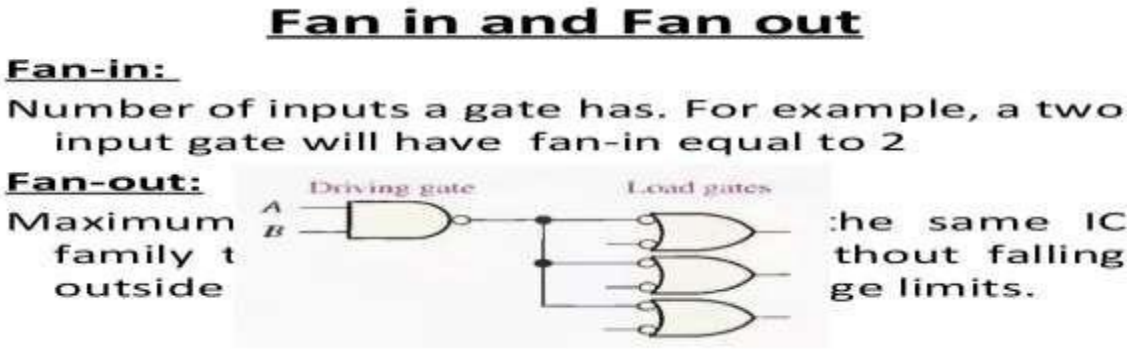
a. NAND

3. Fan-In

Fan in of a logic circuit gives the **maximum number of inputs** that can be connected to the logic circuit without impairing other primary parameters.

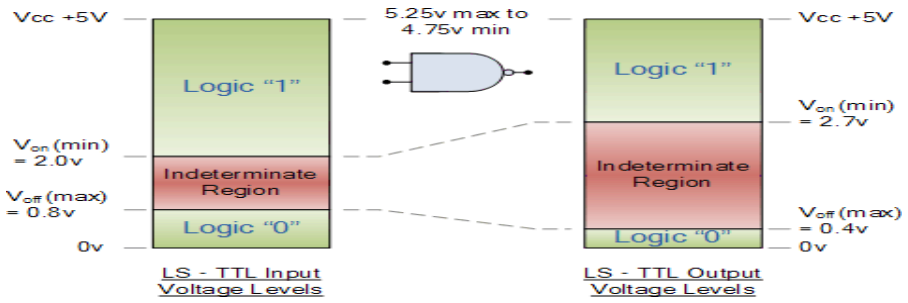
4. Fan-OUT

Fan-out of a logic circuit **is the maximum number of outputs** the circuit may have and still operate properly. The fanout is the limiting factor which determines the number of loads that the given data can drive.



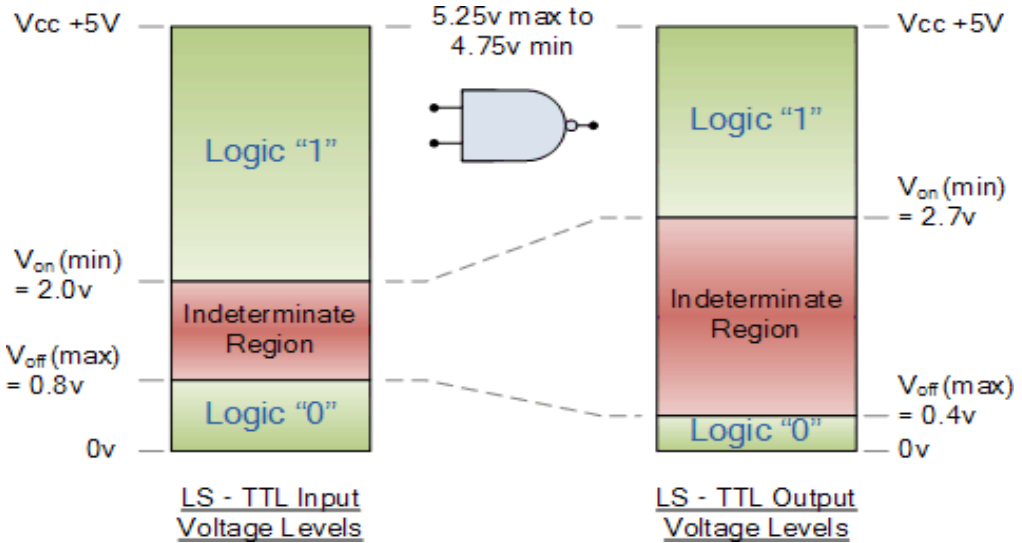
5. Input Logic Level (VIL & VIH)

- If the input voltage level changes without changing the output, this is known as **Input Logic Level** .
- The input is either in logic 0 – low(0V)or logic 1 – High(+5 V)
- some tolerance is allowed to the input voltage.
- Eg: If the input voltage may change from 0V to 0.8V without changing the output level. This voltage of 0.87V is defined as the **Maximum low input voltage** (V_{IL}).
- If the logic 1 may change from + 5V to + 2V without affecting, the output level, then the + 2V is known us the **Minimum high level input voltage** (V_{IH}).



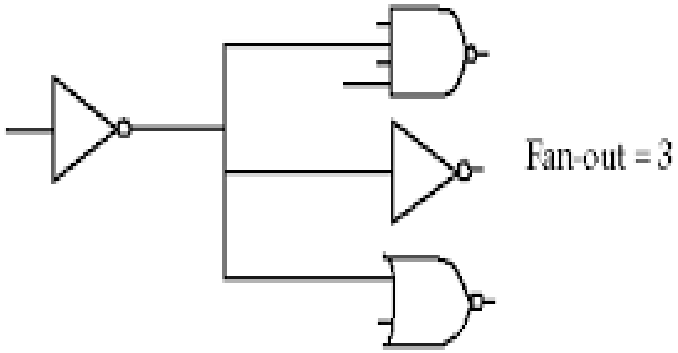
6. Output Logic Level

- The output voltage is at 0V for logic 0 and at 5V for logic 1.
- Eg: In supply voltage variations, voltage drop across resistors etc., so these voltages tend to vary. Thus any voltage say, from 0V to 0.4V is considered as low output.
- Similarly any voltage from 2.7V to 5V is considered as logic 1.
- Thus the worst-case output voltages are the **Maximum low level output voltage** (V_{OL}) and the **Minimum high level output voltages** (V_{OH}).



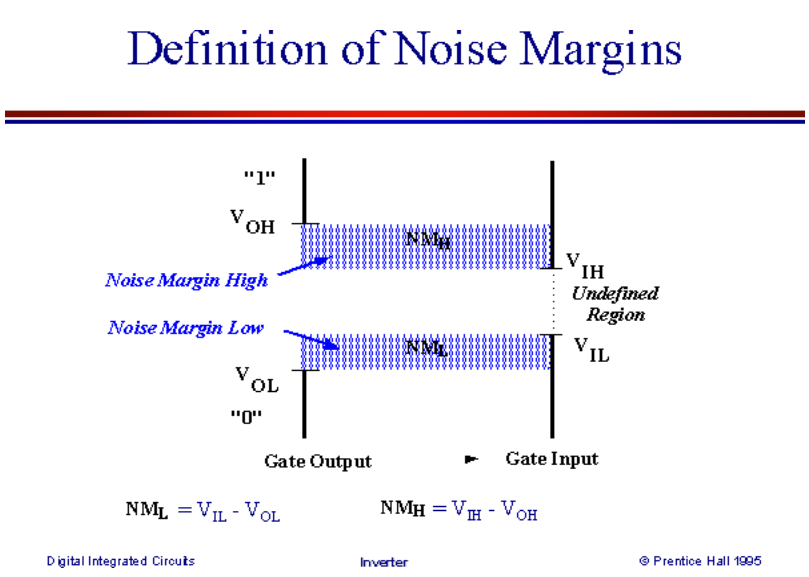
7. COMPATIBILITY(ABILITY TO WORK WITH ANOTHER)

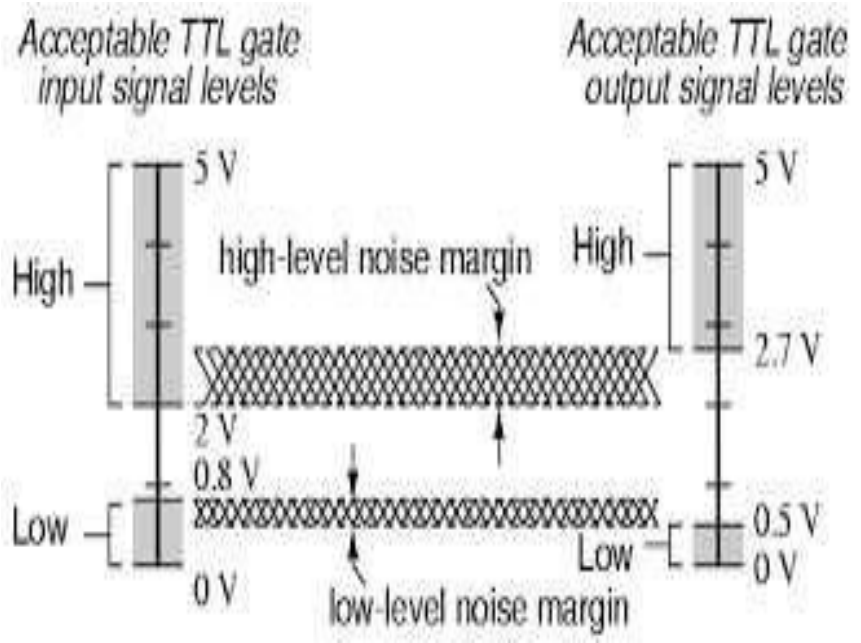
- Compatibility is defined as the **ability of one device to drive the input of another device**.
- If the output of one device is connected to the input of another device, for both the devices the the Input Logic Level and Output Logic Level must be same, then these two devices are compatible .



8. Noise Margin

- There is a minimum permissible variation between the **drive device and the load device** this difference is known as the noise margin.
- As long as the noise level of any stray interference picked by the various leads of the device is within this value of 0.4V the input of the load device is not affected





9. Speed – Power Product

- It is specified by the manufacture as a measure of the performance of a logic circuit based on the product of the propagation delay time and the power dissipation at a specified frequency.
- It is expressed in the units of joules (J).

Speed-Power Product

- Desirable properties:
  - Short propagation delays (high speed)
  - Low power dissipation
- Speed-power product measures the combined effect.

Review of Specification of Digital IC's

1. **Power Dissipation**
2. **Propagation Delay**
3. **Fan-In**
4. **Fan-Out**
5. **Input Logic Level**
6. **Output Logic Level**
7. **Compatibility**
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9. **Speed – Power Product**

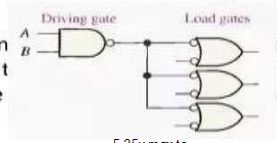
Fan in and Fan out

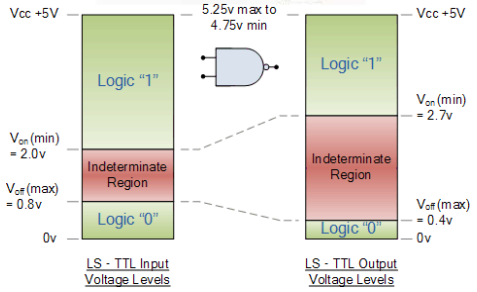
Fan-in:

Number of inputs a gate has. For example, a two input gate will have fan-in equal to 2

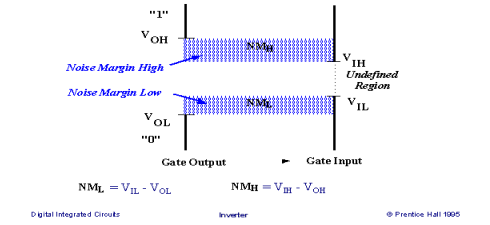
Fan-out:

Maximum :he same IC family t thout falling outside ge limits.





Definition of Noise Margins

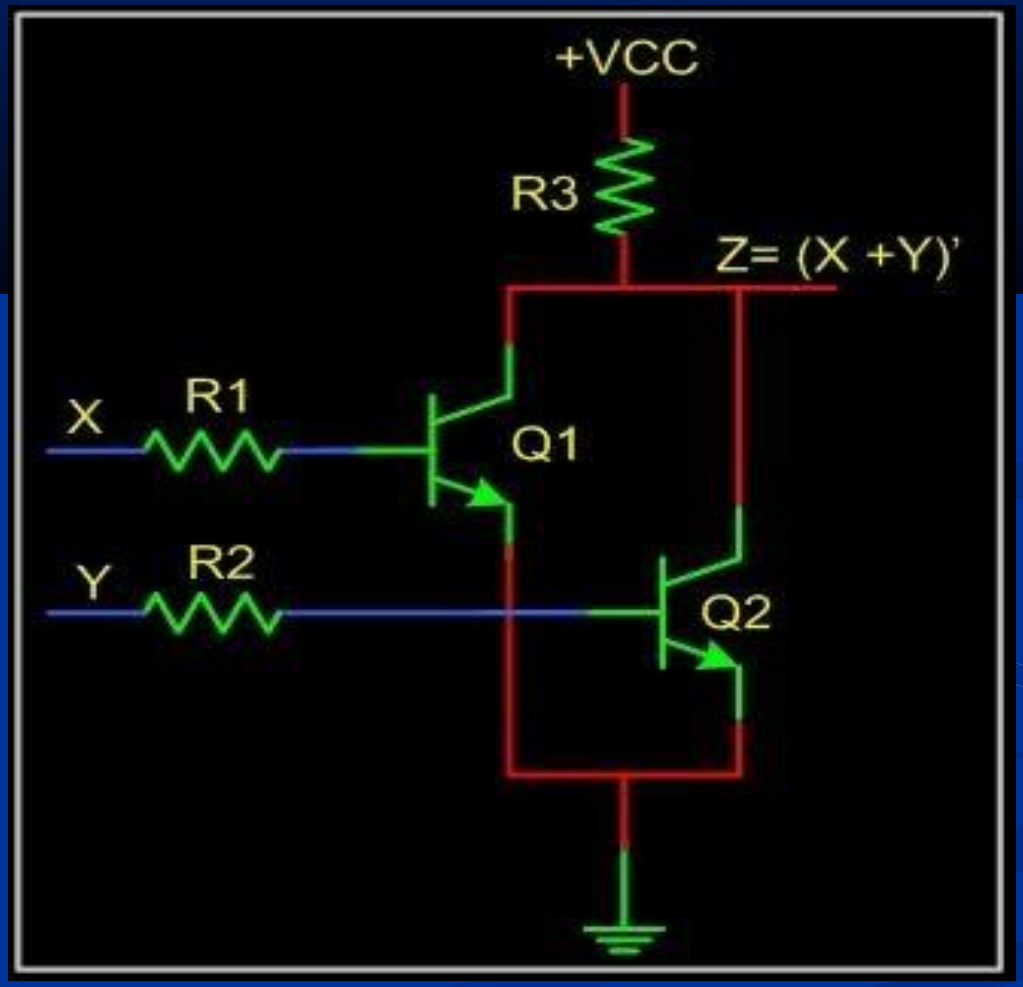


Resistor Transistor Logic

- RTL is the first logic family which is not available in monolithic form.
- The basic circuit of the RTL logic family is the NOR.
- Each input is associated with one resistor and one transistor.

- The collector of the transistor are tied together at the output
- The voltage levels for the circuit are 0.2v for the low level and from 1 to 3.6v for the high level

CIRCUIT DIAGRAM



Truth Table

A	B	Y=A+B
0	0	1
0	1	0
1	0	0
1	1	0

Working:

- **If any input is high**. The corresponding transistor is driven into saturation and the output goes low, regardless of the states of the other transistor.

- **If all inputs are low**. Then all transistor are in cutoff state and the output of the circuit goes high.

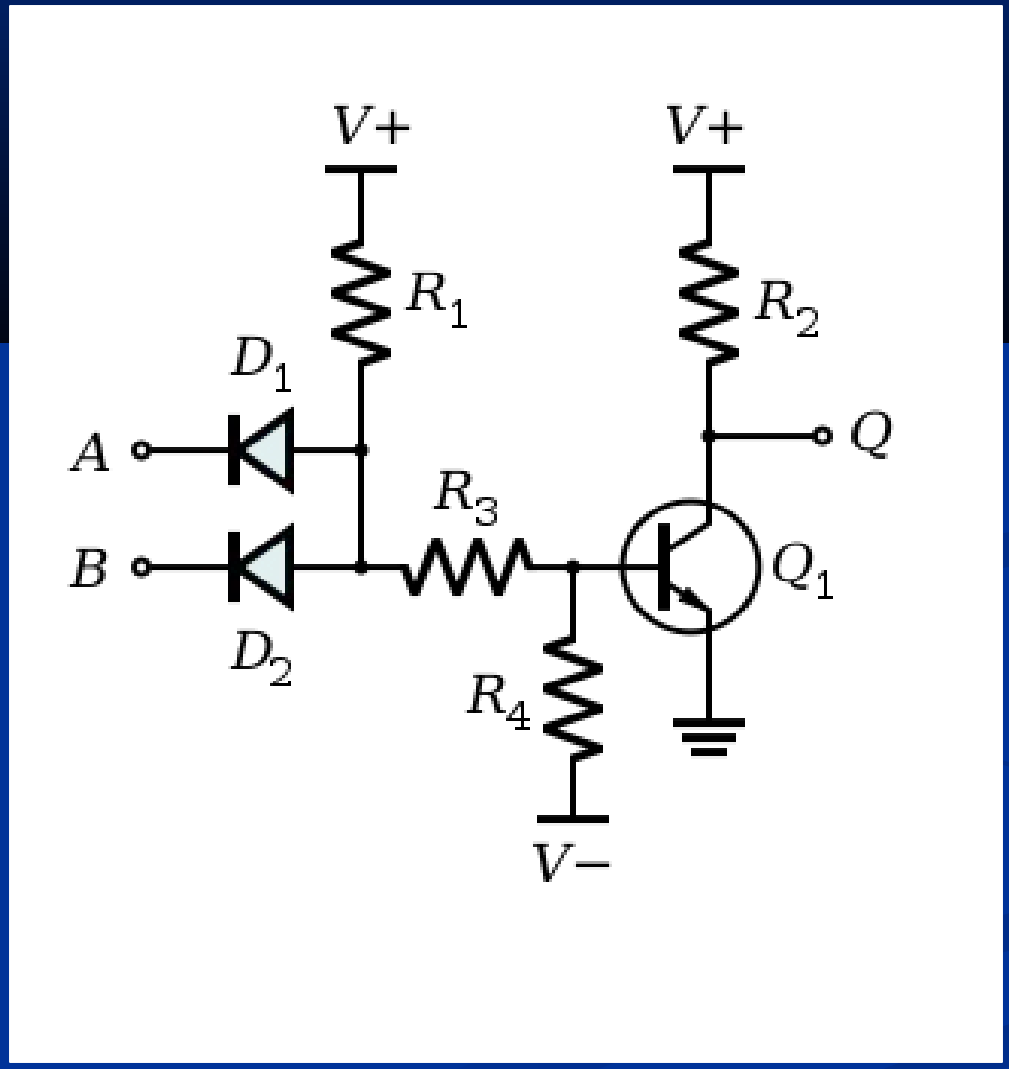
Characteristics :

- It has a fan-out of 5.
- Propagation delay is 25 ns.
- Power dissipation is 12 mw.
- Noise margin for low signal input is 0.4 v.
- Poor noise immunity.
- Low speed.

Diode Transistor Logic(DTL)

- DTL was first commercial available IC logic family in 53/73 series.
- The basic circuit in the DTL logic is the NAND gate.
- Each input associated with one diode.
- The diode and resistor form an AND gate.
- The transistor services as a NOR gate

circuit diagram



Truth table

0	0	1
0	1	1
1	0	1
1	1	0

working :-

If any input is low:-

- The corresponding diode conducts current through V_{cc} and resistor into the input node.

- The voltage at point p is equal to the input voltage + diode drop.

- This is a insufficient voltage for conduction of a transistor.
- Since the voltage at point p is 0v then the transistor is cut off state and the output is logic 1.

If all inputs are high:-

- The transistor is driven into saturation region.
- The voltage at point p is high.
- Hence the output is low.

characteristics :-

- It has fan-out of 8.
- It has high noise immunity.
- Power dissipation is 12mw.
- Propagation delay is average 30ns.
- Noise margin is about 0.7V.

Transistor Transistor Logic(TTL)

- It can perform many digital function and have achieved the most popularity.
- TTL IC are given the numerical designation as 5400 and 7400 series
- The basic circuit of TTL with totem pole output stage is NAND gate

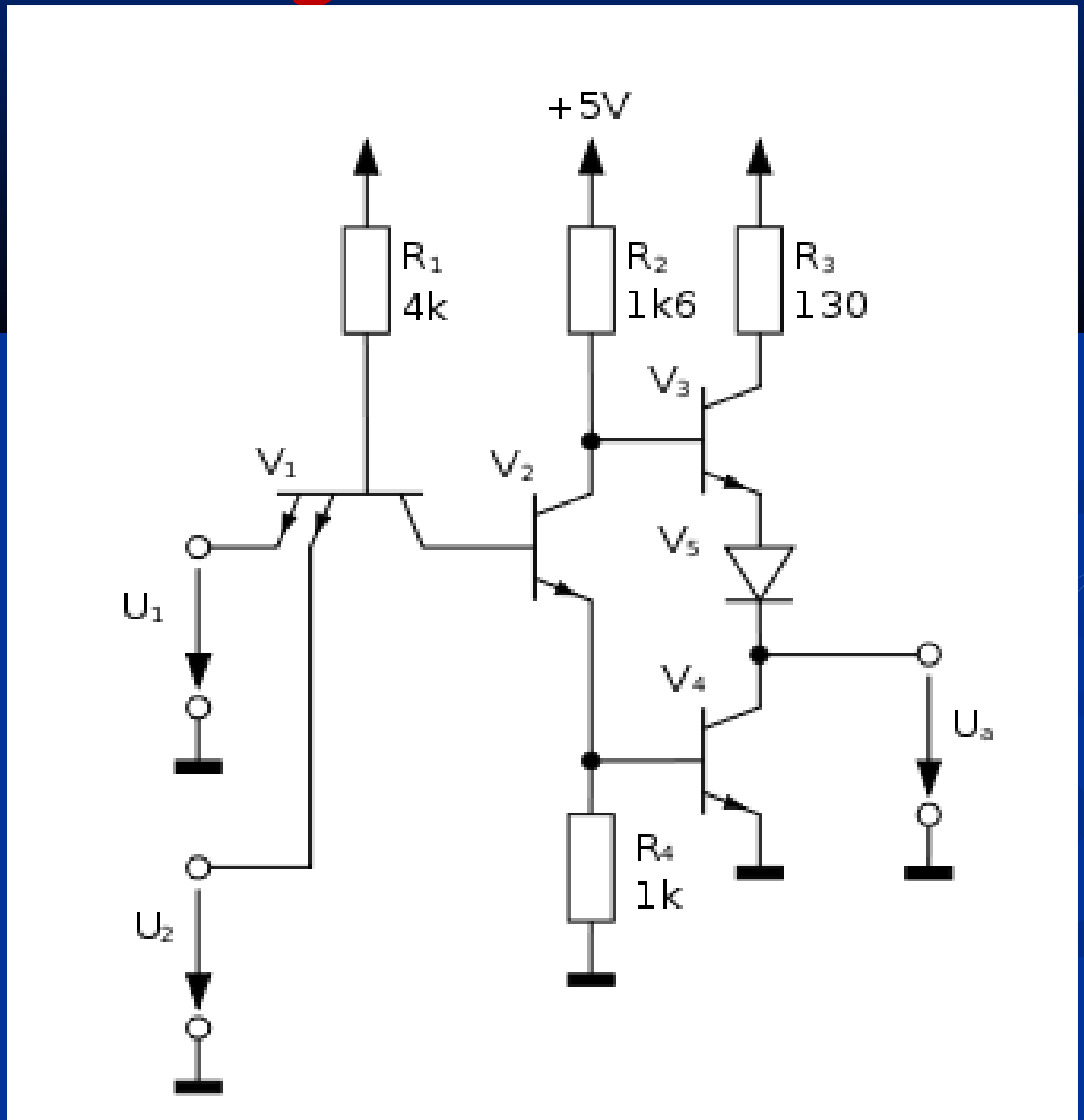
- TTL uses a multi-miter transistor at the input and is fast saturation logic circuit.
- The output transistor Q3 and Q4 form a totem-pole connection.

- This extra output stage is known as totem-pole stage because three output components Q3 and Q4 and Diode are stacked on one another.

- This arrangement will increase the speed the speed of operation and also increase output current capability.

- The function of diode in this circuit prevent both Q3 and Q4 being turned ON simultaneously The function of diode in this circuit prevent both Q3 and Q4 being turned ON simultaneously

Circuit Diagram



TRUTH TABLE

A	B	$Y=\overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

Working:-

- A=0,B=0;A=1,B=0;A=0,B=1;
- ➢ The emitter base junction of Q1 turns on.

- ➢ The collector potential of Q1 falls to 0v,then Q2 turns off.
- ➢ Therefore, at point M we have 0volt i.e., the base voltage of Q2 is 0volt.

- So that, Q2 is also turns off.

- But at the same time we have L=+V_{CC}, this voltage is applied on the base of Q4
- As a result transistor Q3 is turned ON.
- Therefore, the output voltage is given by

V_0=+V_{CC}-[Voltage drop in R4+drop in diode ‘D’]

- A=1,B=1;

➢ When both input are high then emitter base junction of transistor Q1 becomes reverse bias. Hence Q1 is turned off.

➢ However its collector base junction is forward bias, supplying base current to the transistor Q2. Hence Q2 turns ON.

➢ As a result collector potential of Q2 becomes “0” volts.

- Now if L=0volt is applied to the base of Q3, it is turns off .
- At the same time Q4 is turn ON. Then its collector potential nearly equal to 0volts.
- Hence the output is low or logic o.

characteristics:-

- TTL has greater speed than DTL.
- Less noise immunity.
- Power dissipation is 10mw.
- It has fan-in of 6 and fan-out of 10.
- Propagation time delay is 5-15nsec.

EMITTER COUPLED LOGIC GATE(ECL)

- ECL is non saturated digital logic family.
- The output of ECL provides OR and NOR function.
- Each input is connected to the base of transistor.

- The circuit consists of three parts.

  1.differential input amplifier.

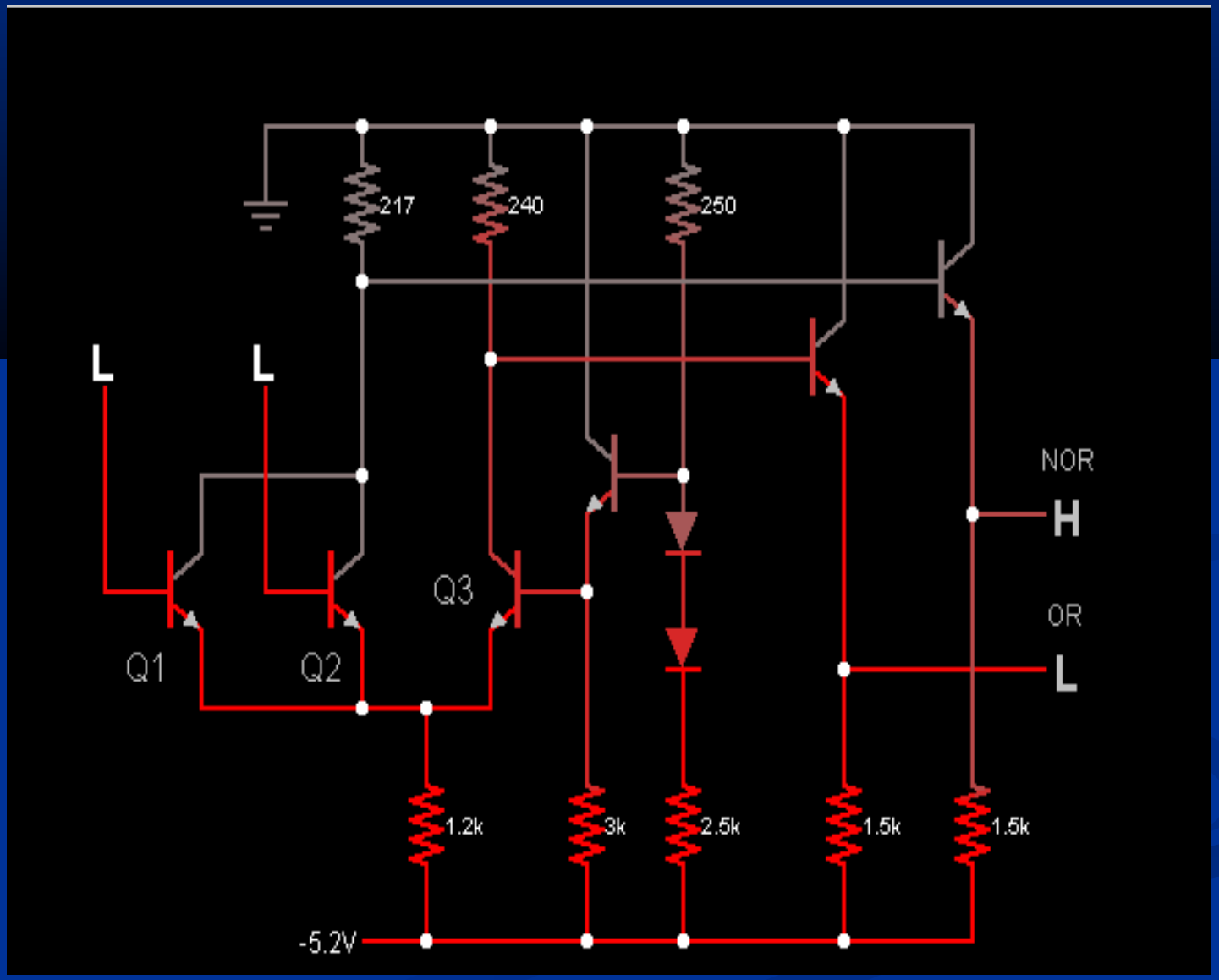
  2.Internal temperature and voltage compensated bias network.

  3.emittor follower output.

- The emitter output requires a pull down resistor for current flow.

- In this logic family we consider the logic 0 as -1.6v and logic 1 as -0.8v.

Circuit Diagram



Truth Table

A	B	$\overline{Y=A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

working:-

- A=0,B=0;
- If all inputs are at low level(-1.6v),the transistor are turn OFF and Q3 conducts .
- Then at point L the potential is 0volts is applied to the base of Q5,it is to be turn OFF.
- So, the output of OR gate is logic ‘0’.

- At the same time , the potential at point M= vcc is applied to the base of Q6,it is to be turn ON.
- So, the output of NOR is at logic 1.

- A=0,B=0,A=0,B=1,A=1,B=0;
  - The corresponding transistor is turned ON and Q3is turned OFF.
  - Because its voltage needs at least 0.6v to start conduction on.
  - An input of -0.8v causes the transistor to conduct and apply -1.6v on the remaining emitters

- Therefore,Q3 is cut off. The voltage in resistor R2 flows into the base of Q5(L=V_{cc}) then Q5 is turned ON.

- The output is at logic 1.

- At the same time, at point M the voltage is 0v is applied to the base of the transistor Q6,it is to be turns off. So, the NOR output is logic 0.

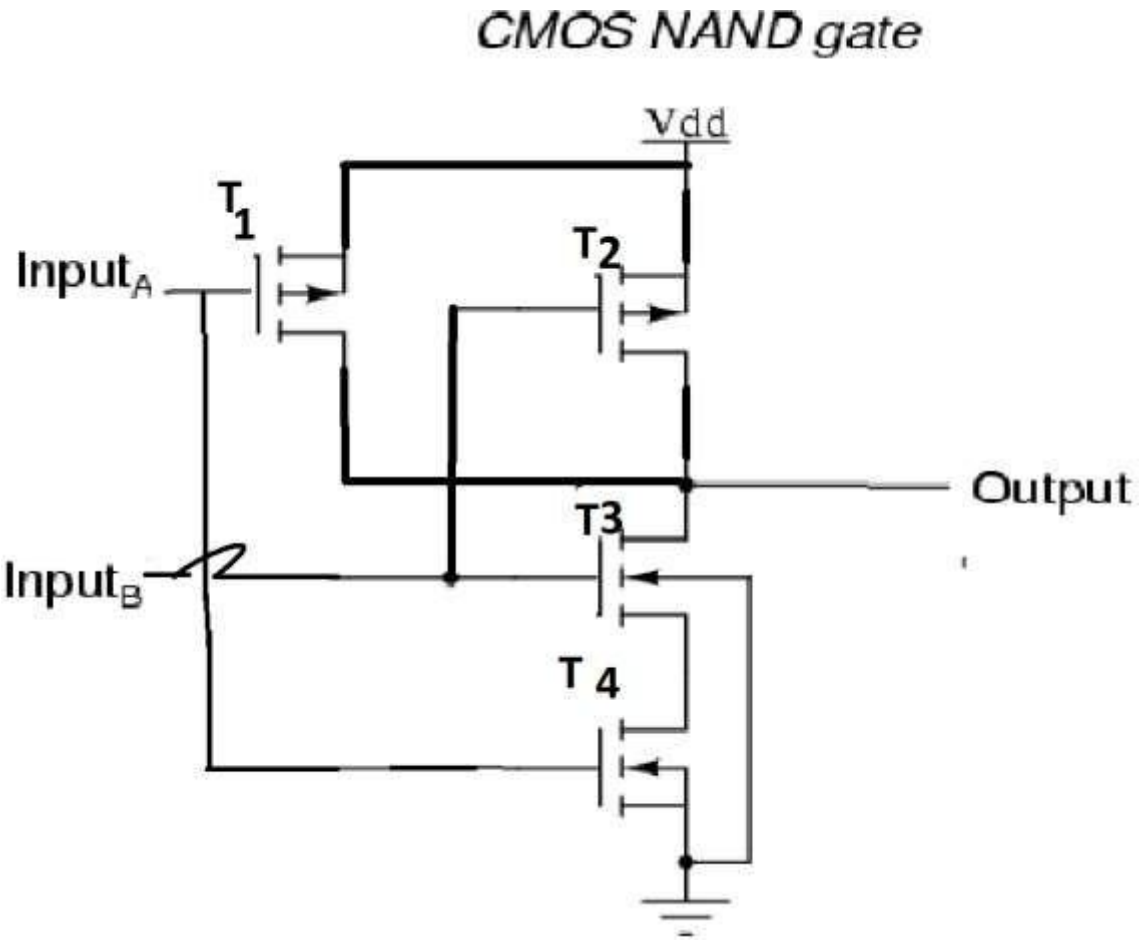
Characteristics :-

- Propagation delay is very LOW(<1ns)
- ECL is fastest logic family.
- ECL circuit usually operate with –Ve supplies (+Ve terminal is connected to ground).

MOS/ CMOS CIRCUIT

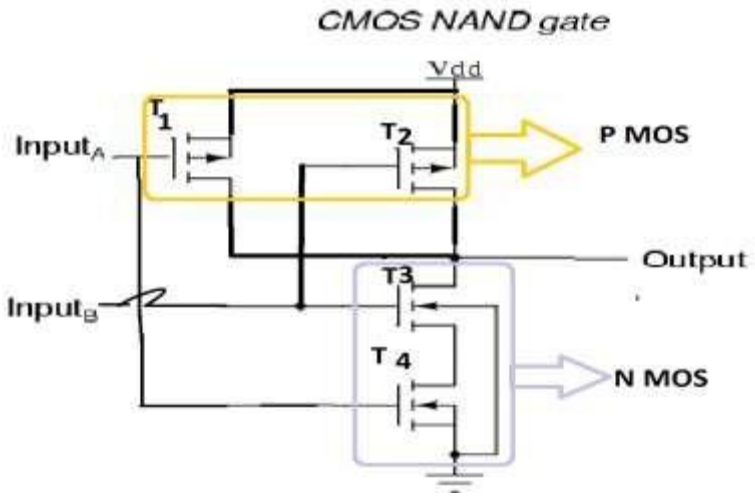
- Metal Oxide Semiconductor(MOS) field effect transistor. There are 3 types
  - P MOS- P- Channel MOSFET – slowest
  - N MOS – N Channel MOSFET – Microprocessor & Memories
  - C MOS (Complementary MOS) – both N& P Channel
    - ADVANTAGES:
      - LOW POWER DISSIPATION
      - LOW NOISE
      - HIGH FAN OUT
      - HIGH SWITCHING SPEED
      - BETTER COMPATIBILITY

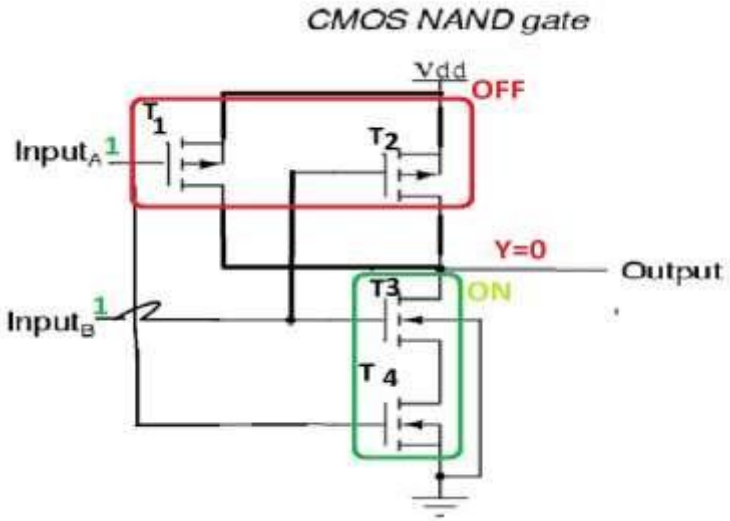
CMOS NAND GATE



CMOS NAND GATE OPERATION

- Complementary MOSFET
- T1 & T2 are p-channel MOSFET
- T3 & T4 are n-channel MOSFET
- If inputs are high ‘1’ then p-channel MOSFET (T1 & T2 – OFF), n-channel MOSFET (T3& T4 – ON), so the output is low.

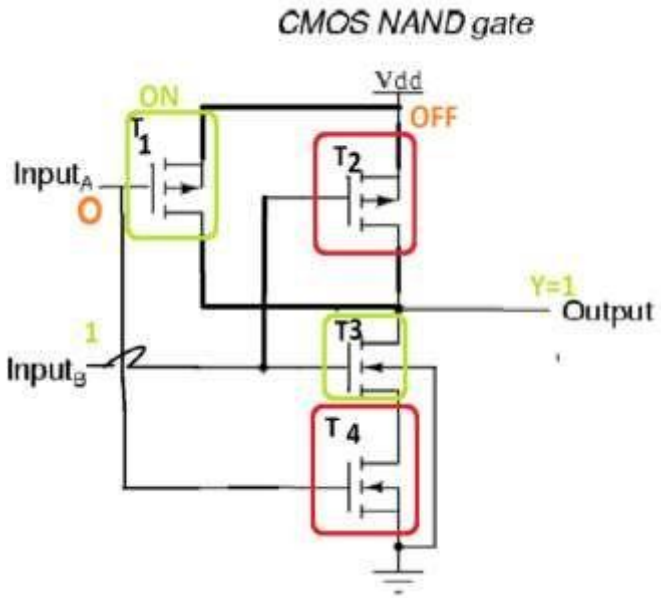


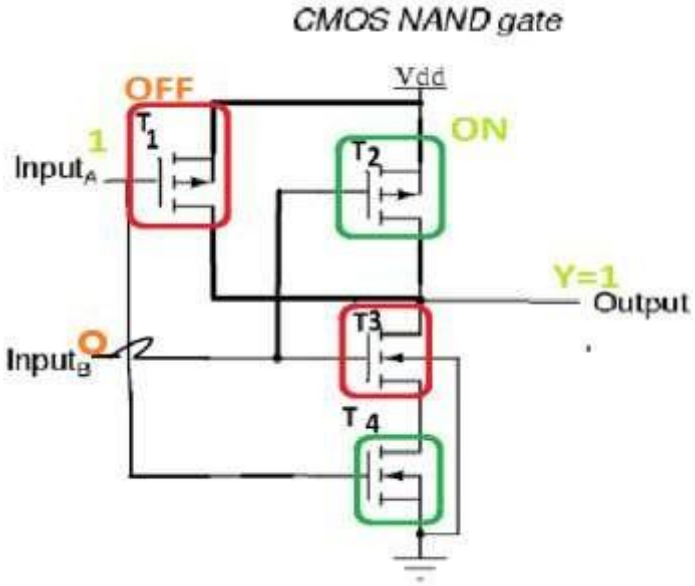


CMOS NAND GATE OPERATION

- If any one of the input is high then the pmos transistor is OFF & its Combinational nmosTransistor is On
- For Eg:

INPUT	T1	T2	T3	T4	OUTPUT
0,0	ON	ON	OFF	OFF	1/HIGH
0,1	ON	OFF	ON	OFF	1/HIGH
1,0	OFF	ON	OFF	ON	1/HIGH
1,1	OFF	OFF	ON	ON	0/ LOW



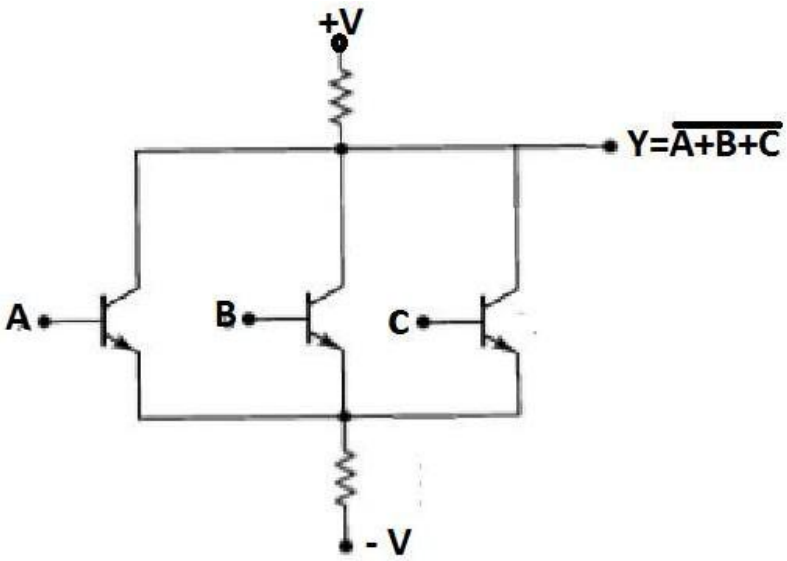


9. EMITTER COUPLED LOGIC(ECL)

- ECL is the **fastest** among all logic families
- The basic component is current switch or difference amplifier with **out-of phase** output .
- This reason ECL is known as Current Mode Logic(CML)
- Transistor operates on Non- saturated at limited collector current, so the emitter coupling is used, it doesn't allow transistor to saturate.
- ADV: [1]. So switching speed is high, [2]. propagation delay is >3ns and [3]High Fan – in & out.
- DIS: [1] Highest power dissipation [2] additional reference voltage source. so it is used in **Superfast computing.**

9. ECL NOR GATE:

- OPERATION:
- If one of the input or all the input are high then the output is low because one or more transistor conducts.
- Output is high when all input is low



10. Comparison of TTL, CMOS & ECL logic family

S.NO	CHARECERIZATION	TTL	CMOS	ECL
1	GATES	NAND	NAND/NOR	NOR
2	Noise ImmunityVin (V)	0.50	1.50	0.16
3	Fan out Fout	>10	>10	>10
4	Fan in Fin	12 to 14	>10	>10
5	Propagation Delay tpd (ns)	15	15	< 3
6	Power Dissipation Pd (mw)	0.1	175	0.001

THANK YOU